PATENT APPLICATION

Sheet 1 of 4

FORM PTO-1449 LIST OF PATENTS AND PUBLICATIONS FOR APPLICANT'S INFORMATION DISCLOSURE STATEMENT (Use several sheets if necessary)	ATTY. DOCKET NO. 200300182-1	APPLICATION NO. 10698271	CONFIRMATION NO.
	APPLICANT Boon S ong Ang et al.		
	FILING DATE	GROUP	

REFERENCE DESIGNATION **U.S. PATENT DOCUMENTS**

EXAMINER INITIAL		DOCUMENT NUMBER	PUBLICATION DATE	NAME	Pages, Columns, Lines Where Relevant Passages or Figures Appear
DC	1A	6,204,690	Mar. 20, 2001	Young et al.	
DC	1B	6,243,851	Jun. 5, 2001	Hwang et al.	
DC	1C	6,292,022	Sep. 18, 2001	Young et al.	
DC	1D	6,553,395	Apr 22, 2003	Marshall et al.	
DC	1E	6,353,841	Mar. 5, 2003	Marshall et al.	
	1F				
	1G				
	1H				
	1I				
	1J				
	1K				

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	PUBLICATION DATE	NAME OF PATENTEE OR APPLICANT	Pages/Columns/Lines Where Relevant Passages/Figures Appear	Check if Translation attached
	1L					
	1M					
	1N					
	1O					
	1P					

OTHER REFERENCES (Including Author, Title, Date, Pertinent Pages, etc.)

DC	1Q	V. Kathail, et al., PICO (Program In, Chip Out) : Automatically Designing Custom Computers, IEEE Computer, September 2002, 35(9), pp. 39-47.
DC	1R	S. C. Goldstein, et al., PipeRench: A Reconfigurable Architecture and Compiler, IEEE Computer, April 2000, 33(4), pp. 70-77
DC	1S	S. C. Goldstein, et al., PipeRench: A Coprocessor for Streaming Multimedia Acceleration, In Proceedings of the 26th Annual International Symposium on Computer Architecture, 1999, pp. 28-39.

EXAMINER	DATE CONSIDERED
David D. Ang	2/18/05

FORM PTO-1449 LIST OF PATENTS AND PUBLICATIONS FOR APPLICANT'S INFORMATION DISCLOSURE STATEMENT (Use sev ral sheets if necessary)	ATTY. DOCKET NO. 200300182-1	APPLICATION NO. 10/698,271	CONFIRMATION NO.
	APPLICANT Bo n Seong Ang t al.		
	FILING DATE	GROUP	

REFERENCE DESIGNATION **U.S. PATENT DOCUMENTS**

EXAMINER INITIAL		DOCUMENT NUMBER	PUBLICATION DATE	NAME	Pages, Columns, Lines Where Relevant Passages or Figures Appear
	2A				
	2B				
	2C				
	2D				
	2E				
	2F				
	2G				
	2H				
	2I				
	2J				
	2K				

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	PUBLICATION DATE	NAME OF PATENTEE OR APPLICANT	Pages/Columns/Lines Where Relevant Passages/Figures Appear	Check if Translation attached
	2L					
	2M					
	2N					
	2O					
	2P					

OTHER REFERENCES (including Author, Title, Date, Pertinent Pages, etc.)

OC	2Q	V. Betz and J. Rose, Effect of the Prefabricated Routing Track Distribution on FPGA Area-Efficiency, IEEE Transactions on VLSI, Sept. 1998, 6(3), pp. 445-456.
OC	2R	Emre Özer, Sanjeev Banerjia, and Thomas M. Conte, Unified Assign and Schedule: A New Approach to Scheduling for Clustered Register File Microarchitectures, In Proceedings of the 31th Annual International Symposium on Microarchitecture (MICRO-31), Dallas, Texas, 1998, pp. 308-315.
OC	2S	M.C. Papaefthymiou, Understanding Retiming Through Maximum Average-Delay Cycles, Mathematical Systems Theory, 1994, 1(27), pp. 65-84.

EXAMINER	DATE CONSIDERED
David D. Chung	2/18/05

FORM PTO-1449 LIST OF PATENTS AND PUBLICATIONS FOR APPLICANT'S INFORMATION DISCLOSURE STATEMENT (Use several sheets if necessary)	ATTY. DOCKET NO. 200300182-1	APPLICATION NO. 10698271	CONFIRMATION NO.
	APPLICANT Bo n Seong Ang t al.		
	FILING DATE	GROUP	

REFERENCE DESIGNATION **U.S. PATENT DOCUMENTS**

EXAMINER INITIAL		DOCUMENT NUMBER	PUBLICATION DATE	NAME	Pages, Columns, Lines Where Relevant Passages or Figures Appear
	3A				
	3B				
	3C				
	3D				
	3E				
	3F				
	3G				
	3H				
	3I				
	3J				
	3K				

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	PUBLICATION DATE	NAME OF PATENTEE OR APPLICANT	Pages/Columns/Lines Where Relevant Passages/Figures Appear	Check if Translation attached
	3L					
	3M					
	3N					
	3O					
	3P					

OTHER REFERENCES (including Author, Title, Date, Pertinent Pages, etc.)

DC	3Q	J. Babb, R. Tessier, and A. Agarwal, Virtual Wires: Overcoming Pin Limitations in FPGA-based Logic Emulators, In Proceedings of the IEEE Workshop on FPGAs for Custom Computing Machines, Los Alamitos, CA 1993, pp. 142-151.
DC	3R	J.S. Rose and S. Brown, Flexibility of Interconnection Structures for Field-Programmable Gate Arrays, IEEE JSSC, March 1991, 26(3), pp. 277-282.
DC	3S	S. Note, et al., Cathedral III: Architecture driven high-level synthesis for high throughput DSP applications, In Proceedings of the 28th ACM/IEEE Design Automation Conference, DAC 91, San Francisco, CA, 1991, pp. 597 - 602.

EXAMINER	DATE CONSIDERED
David D. Cheng	2/18/05

FORM PTO-1449 LIST OF PATENTS AND PUBLICATIONS FOR APPLICANT'S INFORMATION DISCLOSURE STATEMENT (Use several sheets if necessary)	ATTY. DOCKET NO. 200300182-1	APPLICATION NO. 10/698271	CONFIRMATION NO.
	APPLICANT Bo n Seong Ang t al.		
	FILING DATE	GROUP	

REFERENCE DESIGNATION **U.S. PATENT DOCUMENTS**

EXAMINER INITIAL		DOCUMENT NUMBER	PUBLICATION DATE	NAME	Pages, Columns, Lines Where Relevant Passages or Figures Appear
	4A				
	4B				
	4C				
	4D				
	4E				
	4F				
	4G				
	4H				
	4I				
	4J				
	4K				

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	PUBLICATION DATE	NAME OF PATENTEE OR APPLICANT	Pages/Columns/Lines Where Relevant Passages/Figures Appear	Check if Translation attached
	4L					
	4M					
	4N					
	4O					
	4P					

OTHER REFERENCES (including Author, Title, Date, Pertinent Pages, etc.)

DC	4Q	Constantine N. ANAGNOSTOPOULOS, Paul P. K. LEE, Application-Specific Integrated Circuits, The Electronics Handbook, pp. 731-748, CRC Press, Boca Raton FL, 1996.
DC	4R	Bradley K. FAWCETT, Software Development Tools for Field Programmable Gate Array Devices, The Electronics Handbook, pp. 784-793, CRC Press, Boca Raton FL, 1996.
	4S	

EXAMINER	DATE CONSIDERED
Daniel D Chang	2/18/05